Order Number: MC33790/D
Rev. 0, 09/2001

MOTOROLA

MC33790

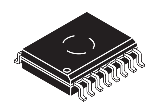
Advance Information

DSI Physical Interface Device

TWO CHANNEL DISTRIBUTED SYSTEM INTERFACE (DSI) PHYSICAL INTERFACE DEVICE

SEMICONDUCTOR TECHNICAL DATA

The MC33790 is a two channel physical layer interface IC for the Distributed Systems Interface (DSI) bus. It is designed to meet automotive requirements. It can also be used in other non–automotive applications. In providing two standard DSI busses, it supports bi–directional communication between the slave and master ICs. Some slave devices derive a regulated 5 volts from the bus which can be used to power sensors, eliminating the need for additional circuitry and wiring.

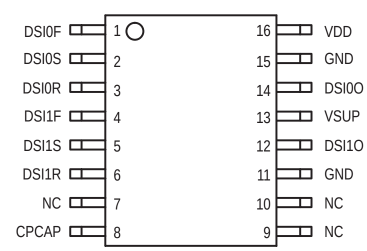


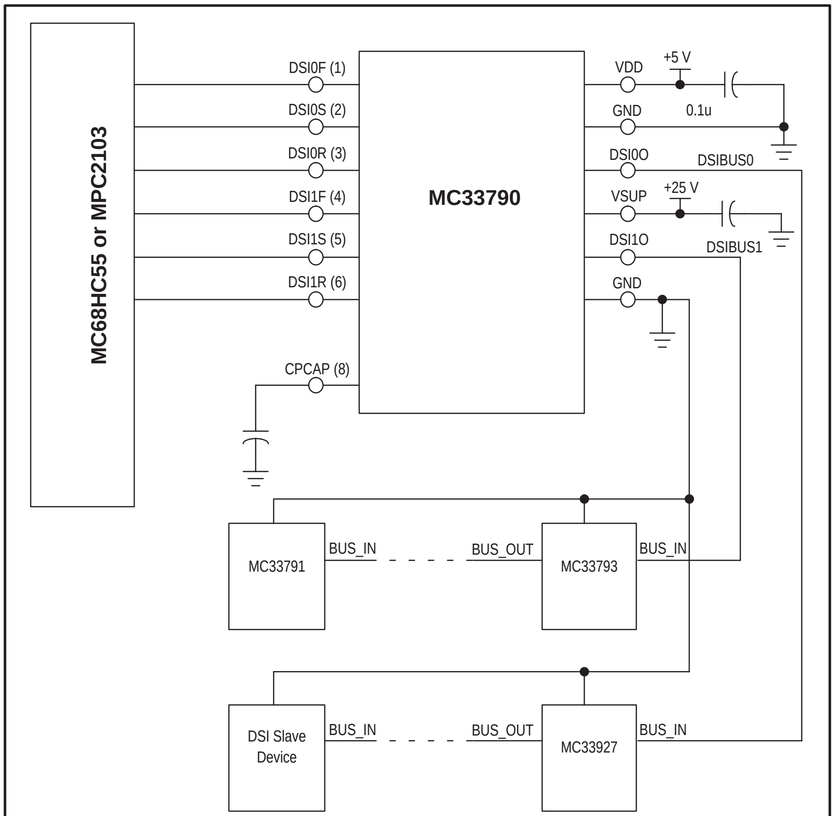
DW Suffix
16–Lead SOIC
Plastic Package
CASE 751G

Features

- Two Independent DSI Busses
- Pinout Matched to MC68HC55 (SPI to DSI Logic)
- Waveshaped Bus Output
- Independent Thermal Shutdown
- 2kV ESD Capability

PIN CONNECTIONS





Simplified Application

ORDERING INFORMATION

Device	Temperature Range	Package
MC33790DW	–40°C to +85°C	SO–16W

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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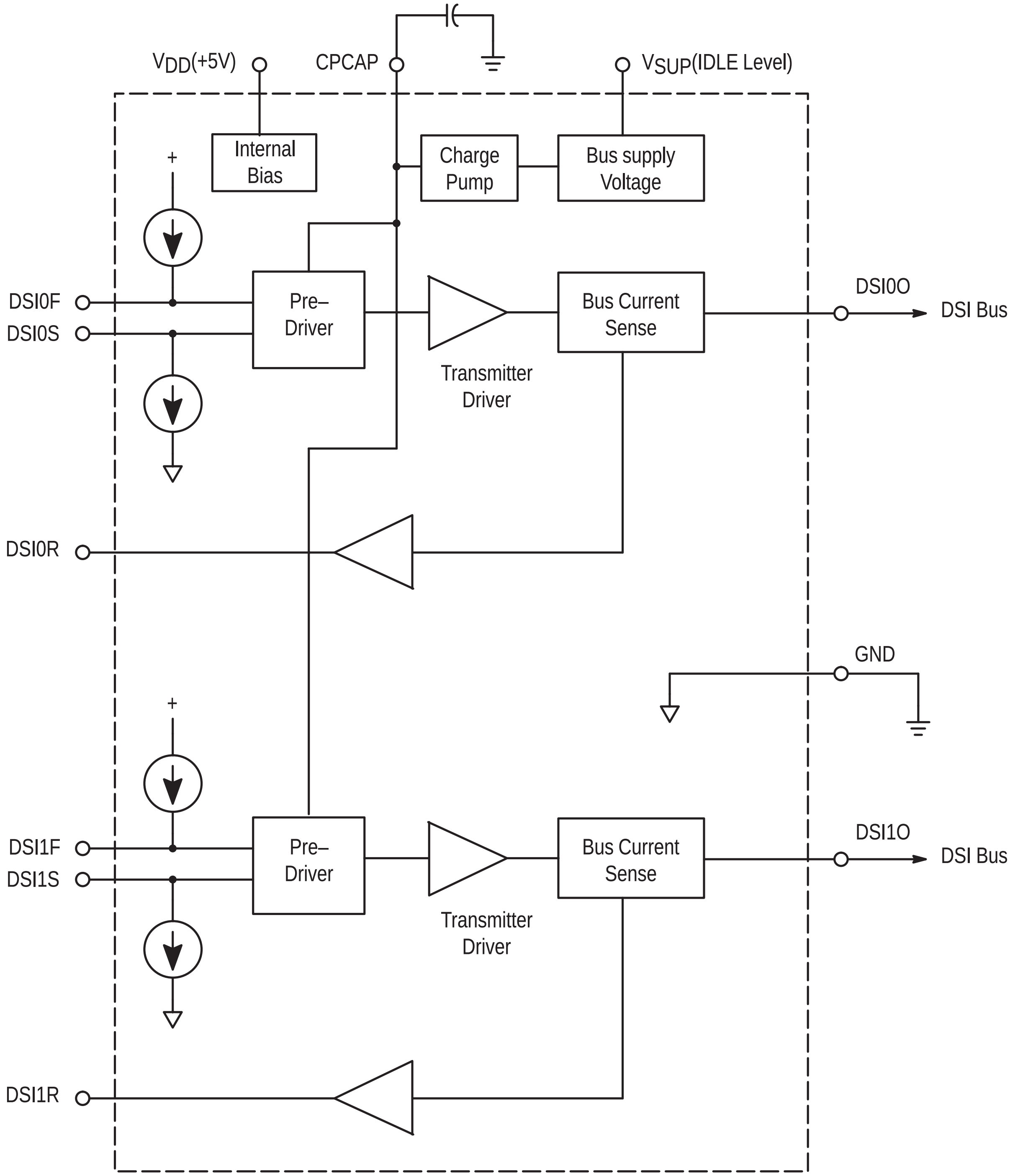


Figure 1. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	DSI0F	This logic input controls the frame output for DSI channel 0 per Table 1.
2	DSI0S	This logic input controls the signalling output for DSI channel 0 per Table 1
3	DSI0R	This logic output provides the return data for DSI channel 0 per Table 1.
4	DSI1F	This logic input controls the frame output for DSI channel 1 per Table 1.
5	DSI1S	This logic input controls the signalling output for DSI channel 1 per Table 1.
6	DSI1R	This logic output provides the return data for DSI channel 1 per Table 1.
7	NC	Unused
8	CPCAP	Charge pump capacitor. Used to store and filter charge pump output.
9	NC	Unused.
10	NC	Unused.
11	GND	Circuit and bus ground return.
12	DSI1O	DSI bus 1 input/output.
13	VSUP	Idle level supply input. The voltage supplied to this pin sets the idle level on the DSI bus.
14	DSI0O	DSI bus 0 input/output.
15	GND	Circuit and bus ground return.
16	VDD	5 volt logic supply input.

MAXIMUM RATINGS (All voltages are with respect to ground unless otherwise noted)

Rating	Symbol	Value	Limit
Supply Voltage Continuous Load Dump – t < 300mS	 V_{SUP} $V_{SUP(t)}$	 –0.5 to 25 40	 V V
Maximum Voltage on Input/Output pins V_{DD} DSIxS, DSIxF, – R = 0 Ω DSIxO – R = 0 Ω		 –0.3 to 5.5 –0.3 to V_{DD}+0.3 –0.3 to V_{SUP}+0.3	 V V V
Operating Temperature	T_A	–40 to +85	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Operating Junction Temperature	T_J	–40 to +150	°C
Lead Temperature (IR Reflow soldering for >60 seconds at >183°C), 10 seconds at >215°C	T_{solder}	230	°C
Continuous Current per Pin	V_{DD} DSIxR V_{SUP}	0 to 10 –2.5 to 5.0 0 to 150	mA mA mA
Thermal Resistance Junction to Ambient	$\varnothing_{JA}$	45	°C/W
Thermal Shutdown	T_{SD}	155 to 190	°C
ESD1 Voltage (All Pins) Human Body Model (Note 1) Machine Model (Note 2)	 V_{ESD1} V_{ESD2}	 ±2000 ±200	 V V

Note 1: ESD1 performed in accordance with the Human Body Model (C_{Zap} = 100pF, R_{Zap} = 1500Ω).
Note 2: ESD2 performed in accordance with the Machine Model (C_{Zap} = 100pF, R_{Zap} = 0Ω).

STATIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{SUP} ≤ 25.0 V, –40°C ≤ TA ≤ 85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY					
I_{SUP} Supply Current / Channel (not including I_{out}) DSIx0 = Idle Voltage, –100 mA < I_{out} < 0mA DSIx0 = Output High Voltage, = I_{out} 12mA DSIx0 = Output Low Voltage, = I_{out} 12mA	 I_{SUPI} I_{SUPH} I_{SUPL}	 – – –		 3.25 6.50 6.50	 mA mA mA
I_{DD} Supply Current / Channel	I_{DD}	–		1.0	mA
BUS TRANSMITTER					
V_{SUP} to DSIxO On Resistance (During Idle) I_{OUT} = –100mA, V_{SUP} = 8V I_{OUT} = –100mA, V_{SUP} = 25V	R_{DSON}	 – –		 10 10	 Ω Ω
Output High Voltage DSIx0 (1mA ≤ Iout ≤ –15mA)	$DSIV_{0H}$	4.175	4.5	4.825	V
Output Low Voltage DSIx0 (–1mA ≤ Iout ≤–15mA)	$DSIV_{OL}$	1.325	1.5	1.675	V
Output High Side Current Limit	I_{CLH}	–100		–200	mA
Output Low Side Current Limit	I_{CLL}	110		220	mA
Input Leakage DSIxO when DSIxF is high and DSIxS is low (0V ≤ DSIxO ≤ min (VSUP, 16.5V))	DSI_{IB}	–200		50	µA
BUS RECEIVER					
Return Current High	I_{RH}	5.0	6.0	7.0	mA
Receiver Low Pass Filter Corner Frequency, Single Pole (Note 3)	f_c	80	100	120	KHz
MICROCONTROLLER INTERFACE					
Logic Input Thresholds DSIxS, DSIxF	V_{ITH}	1.10		2.20	V
Output High Voltage DSIxR pin = –0.5mA	V_{OH}	0.8 * V_{DD}		V_{DD}	V
Output Low Voltage DSIxR pin = 1mA	V_{OL}	0.0		0.2 * V_{DD}	V
Internal Pull–up for DSIxF	I_{IL}	–100		–10	µA
Internal Pull–down for DSIxS	I_{IH}	10		100	µA

Note 3: This parameter assured by design. It is not tested in production.

DYNAMIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{SUP} ≤ 25.0 V, –40°C ≤ TA ≤ 85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
MICROCONTROLLER INTERFACE					
Microcontroller Signal Cycle Time	T_{cyc}	6.6		1000	µs
Microcontroller Signal Low Time	T_{cycL}	2.0		667	µs
Microcontroller Signal High Time	T_{cycH}	2.0		667	µs
Microcontroller Signal Duty Cycle for Logic Zero	DC_{Lo}	30	33	36	%
Microcontroller Signal Duty Cycle for Logic One	DC_{Hi}	60.0	66.7	72.0	%
Microcontroller Signal Slew Time	T_{Slew}	–		500	ns
Frame Start to Signal Delay Time	T_{Dly1}	T_{cyc} – 0.1	T_{cyc}	T_{cyc} + 0.1	µs
Signal End to Frame End Delay Time	T_{Dly2}	2* T_{cyc} /3 – 0.1	T_{cyc}	2* T_{cyc} /3 + 0.1	µs
BUS TRANSMITTER					
Idle to Frame & Frame to Idle Slew Rate, C ≤ 10nF	$t_{slew(FRAME)}$	–	6.0	10.0	V/µs

DYNAMIC ELECTRICAL CHARACTERISTICS (Characteristics noted under conditions 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{SUP} ≤ 25.0 V, –40°C ≤ TA ≤ 85°C, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Signal High to Low & Signal Low to High Slew Rate, C ≤ 10nF	$t_{slew(SIGNAL)}$	3.0	4.5	8.0	V/µs
Data Valid (V_{SUPx} = 25V, C_L ≤ 5nF)					µs
DSIxF low to DSIxO = 5.5V	tDVLD1	2.44		6.90	
DSIxS low to DSIxO = 2.0V	tDVLD2	0.25		1.63	
DSIxS High to DSIxO = 4.0V	tDVLD3	0.25		1.63	

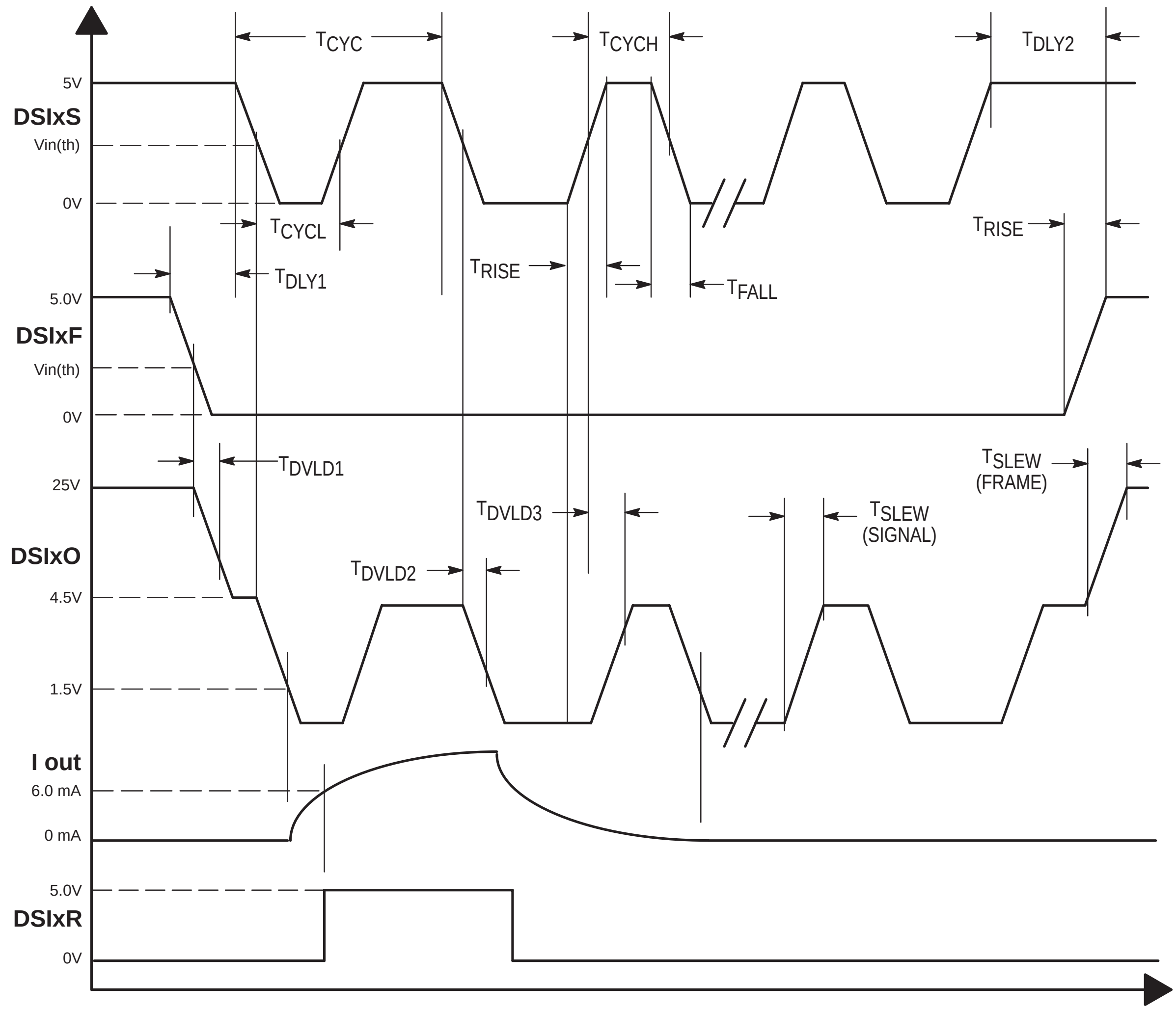


Figure 2. Timing Characteristics

FUNCTIONAL DESCRIPTION

BUS DRIVER AND RECEIVER

The Pre–Driver circuit converts the 0 to 5 volt logic inputs from DSIxF (frame) and DSIxS (signal) to a signal on the DSIxO output as shown in the timing diagrams of Figure 2 and the truth table in Table 1. The Bus Current Sense detects the current being drawn by the device(s) on the bus during signalling (DSIxF = 0). If the current is above a set level, DSIxR will be high, otherwise, it is low.

Table 1 – DSI Bus Truth Table

DSIxF	DSIxS	T_{LIM}	DSIR	DSIxO
0	0	0	Return Data	Low (1.5 V)
0	1	0	Return Data	High (4.5 V)
1	0	0	0	High Impedance
1	1	0	0	Idle ≥ V_{SUP} – 0.5V
X	X	1	1	High Impedance

The DSIxO output is capable of supplying a continuous current of up to 200mA during the Idle state, and a continuous current of 15mA during the transmission state (output low or output high). The current for the idle state is from the supply connected to V_{SUP} and this supply should not be current limited below 250 mA. During idle state, the voltage on the DSI bus will be very close to the V_{SUP} voltage.

Internal thermal shutdown circuitry individually protects the DSIxO outputs from shorts to battery and ground.

Typically, the thermal shutdown occurs between 160°C and 170°C. If the junction temperature rises above this temperature, the output drivers for DSIxO are disabled by the thermal shutdown circuitry. The output drivers remain off until the junction temperature decreases below approximately 155°C, at which time the thermal shutdown circuitry turns off and the outputs are re–enabled. Each DSIxO output shall have a unique thermal sense and shutdown circuit so a short on one channel does not affect another channel.

CHARGE PUMP

The Charge Pump uses on–board capacitors to step the input voltage up to the voltage needed to drive the on–board transmitter FETs. A filter/storage capacitor is connected to CPCAP to hold the stepped up voltage.

INPUT PULL–UPS AND PULL–DOWNS

Internal current pull–ups are used on the DSIxF pins and pull–downs on the DSIxS pins. If these pins are left unconnected, their associated DSI bus will go to the unused (high impedance) state.

APPLICATION INFORMATION

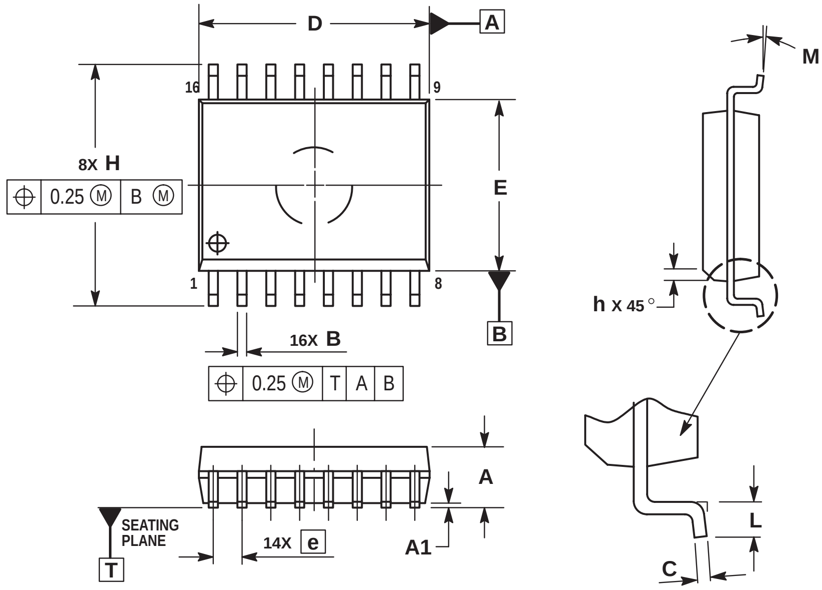
The MC33790 is intended for use in a DSI system. This device supplies the interface between standard logic levels and the voltage and current required for the DSI bus. Two independent DSI busses are supported by this part. The MC33790 does not form the timing for the DSI bus. This is done by logic either embedded in a micro–controller or by the MC68HC55 which uses SPI commands and forms DSI protocol for communications over the DSI bus.

The pins from the MC68HC55 are made to line up with the pins connecting to the MC33790. This includes all the DSInF, DSInS, and DSInR pins.

A capacitor attached to CPCAP serves as a charge reservoir for the gate drive charge pump. This circuit creates a voltage which is higher than the source of the n–channel output transistor. This allows turning on the transistor enough to prevent any significant voltage drop across it. The rest charge pump electronics are completely self contained on the IC.

PACKAGE DIMENSIONS

DW SUFFIX
PLASTIC PACKAGE
16–LEAD SOIC WIDE BODY
CASE 751G–04
ISSUE C



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.40	1.00
M	0 °	7 °

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ASIA / PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852–26668334

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